



Replacement Sheet

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100	101	1	7	1	1	8	1	1
S	Slave Address	WR	A	Data Byte	A	P		

FIG. 1
(Prior Art)

1	7	1	1	1	1	1	1	1
S	Slave Address	RD	WR	A	P			

FIG. 2
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	WR	A	Command Code	A	P		

FIG. 3
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	RD	A	Data Byte	A	P		

FIG. 4
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	RD	A	Command Code	A	P		

FIG. 5
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	RD	A	Data Byte	A	P		

FIG. 6
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	WR	A	Command Code	A	P		

FIG. 7
(Prior Art)

1	7	1	1	8	1	1	1	1
S	Slave Address	WR	A	Command Code	A	Data Byte Low	A	Data Byte High

FIG. 8
(Prior Art)

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*FIG. 9
(Prior Art)*

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	WR	A	Command Code	A	Data Byte	A	PEC	A	P

*FIG. 10
(Prior Art)*

1	7	1	1	8	1	1	7	1	1	8
S	Slave Address	WR	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC

*FIG. 11
(Prior Art)*

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	WR	A	Command Code	A	Sr	Slave Address	RD	A	Data Byte	A	P

*FIG. 12
(Prior Art)*

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	WR	A	Command Code	A	Sr	Slave Address	RD	A	Data Byte	A	...

8	1	1
PEC	A	P

*FIG. 13
(Prior Art)*

8	1	1
Data Byte High	A	P

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FIG. 14	1	7	1	1	8	1	1	7	1	1	8	1
(Prior Art)	S	Slave Address	W/R	A	Command Code	A	S	Slave Address	RD	A	Data Byte Low	A
	8	1	8	1	1							
	Data Byte High	A	PEC		A	P						

FIG. 15	1	7	1	1	8	1	8	1	8	1
(Prior Art)	S	Slave Address	WR	A	Command Code	A	Data Byte Low	A	Data Byte High	A
	1	7	1	1	7	1	8	1	1	1
	SR	Slave Address	RD	A	Data Byte Low	A	Data Byte High	A	P	1

FIG. 16 (Prior Art)		S	Slave Address	WR	A	Command Code	A	Data Byte Low	A	Data Byte High	A	...
SR	Slave Address	RD	A	Data Byte Low	A	Data Byte High	A	PEC	A	P		
1	7	1	1	8	1	8	1	8	1	8	1	
1	7	1	1	8	1	8	1	8	1	8	1	

FIG. 17
(Prior Art)

S	Slave Address	WR	A	Command Code	A	Byte Count=N	A	Data Byte 1	A	...
8	1	...	8	1	1	8	1	8	1	...
Data Byte 2		A	...	Data Byte N		A	P			

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The timing diagram illustrates the sequence of bytes transmitted between a Master and a Slave. The bytes are transmitted sequentially from left to right:

- Slave Address:** A 7-bit byte followed by a stop bit (A).
- WR:** A 1-bit byte.
- Command Code:** An 8-bit byte.
- Byte Count=N:** An 8-bit byte.
- A:** A stop bit.
- Data Byte 1:** An 8-bit byte.
- ...:** A separator symbol indicating continuation.
- Data Byte 2:** An 8-bit byte.
- A:** A stop bit.
- ...:** A separator symbol indicating continuation.
- Data Byte N:** An 8-bit byte.
- A:** A stop bit.
- PEC:** An 8-bit byte.
- A:** A stop bit.
- P:** A final stop bit.

FIG. 20
(Prior Art)

Slave Address	WR	A	Command Code	A	Sr	Slave Address	RD	A	Byte Count=N	A	...
8	1	8	1	1	7	1	1	8	1	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	...	PEC	A	P	1

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1	7	1	1	8	1	8	1	8	1	8	1
S	Slave Address	WR	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	Data Byte 2	A
8	1	1	7	1	1	8	1	8	1	8	1
Data Byte M	A	Sr	Slave Address	RD	A	Byte Count=N	A	Data Byte 1	A	...	
8	1	...	8	1	1						
Data Byte 2	A	...	Data Byte N	A	P						
						1					

*F/G. 21
(Prior Art)*

1	7	1	1	8	1	8	1	8	1	8	1
S	Slave Address	WR	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	Data Byte 2	A
8	1	1	7	1	1	8	1	8	1	8	1
Data Byte M	A	Sr	Slave Address	RD	A	Byte Count=N	A	Data Byte 1	A	...	
8	1	...	8	1	1						
Data Byte 2	A	...	Data Byte N	A	PEC	A	P				
						1					

*F/G. 22
(Prior Art)*